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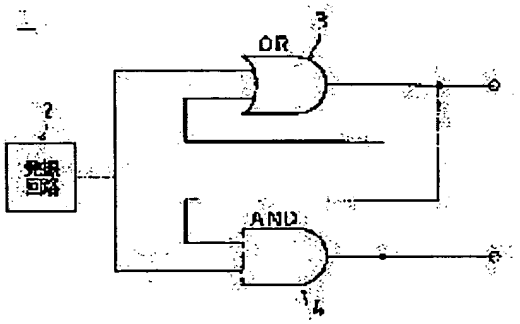
(54) SWITCHING ELEMENT DRIVING CIRCUIT

(57)Abstract:

PURPOSE: To provide a switching element driving circuit for surely preventing a state in which two switching elements are simultaneously turned on.

CONSTITUTION: This switching element driving circuit 1 is provided with an oscillation circuit 2 for generating width-controlled control signals, an OR circuit 3 for outputting first driving signals for driving one of the switching elements and an AND circuit 4 for outputting second driving signals for driving the other switching element. The first driving signals of the OR circuit 3 are generated by 0Ring the control signals of the oscillation circuit 2 and the second driving signals of the AND circuit 4 and the second driving signals of the AND circuit 4 are generated by ANDing the control signals of the oscillation circuit 2 and the first driving signals of the OR circuit 3.



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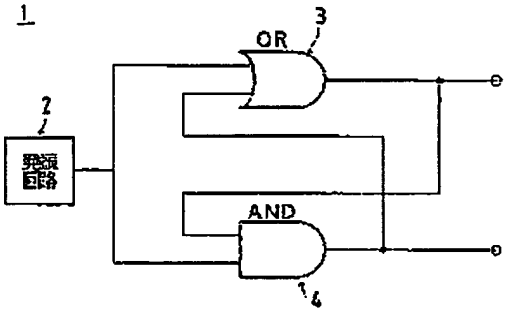
(54)【発明の名称】　スイッチング素子駆動回路

(57)【要約】
【目的】２つのスイッチング素子が同時にオンする状態を確実に防ぐスイッチング素子駆動回路を提供する。
【構成】このスイッチング素子駆動１は、幅制御された制御信号を発生する発振回路２と、スイッチング素子の一方を駆動する第１の駆動信号を出力する論理和回路３と、スイッチング素子の他方を駆動する第２の駆動信号を出力する論理積回路４と、を備え、論理和回路３の第１の駆動信号は発振回路２の制御信号と論理積回路４の第２の駆動信号とを論理和演算して生成し、論理積回路４の第２の駆動信号は発振回路２の制御信号と論理和回路３の第１の駆動信号とを論理積演算して生成することを特徴とする。



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【特許請求の範囲】

【請求項１】２つのスイッチング素子を交互にスイッチングする同期式のスイッチング素子駆動回路において、幅制御された制御信号を発生する発振回路と、前記スイッチング素子の一方を駆動する第１の駆動信号を出力する論理和回路と、前記スイッチング素子の他方を駆動する第２の駆動信号を出力する論理積回路と、を備え、前記論理和回路の第１の駆動信号は前記発振回路の制御信号と前記論理積回路の第２の駆動信号とを論理和演算して生成し、前記論理積回路の第２の駆動信号は前記発振回路の制御信号と前記論理和回路の第１の駆動信号とを論理積演算して生成することにより、２つのスイッチング素子が同時にオンする状態を防ぐことを特徴とするスイッチング素子駆動回路。

【請求項２】前記論理和回路と前記論理積回路間に遅延回路を設けたことにより、前記スイッチング素子がスイッチするタイミングを調整したことを特徴とする請求項１記載のスイッチング素子駆動回路。

【請求項３】ＤＣ－ＤＣコンバータのスイッチング素子に使用したことを特徴とする請求項１及び請求項２記載のスイッチング素子駆動回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、スイッチング素子駆動回路に関し、例えば、ＤＣ－ＤＣコンバータに用いられるスイッチング素子駆動回路に関する。

【０００２】

【従来の技術】直流電源を入力とし、安定化した直流電圧を出力する降圧チョッパ型のＤＣ－ＤＣコンバータの基本回路を図４に示す。図４において、１１はＤＣ－ＤＣコンバータ、１２は直流入力電源、１３はＭＯＳ形のＰチャンネルＦＥＴ、１４は発振回路、Ｄ１は整流ダイオード、Ｌ１はインダクタンス、Ｃ１はコンデンサ、Ｒ１は負荷を示す。

【０００３】ＤＣ－ＤＣコンバータ１１は、直流入力電源１２の直流電圧を発振回路１４の駆動信号を印加したＰチャンネルＦＥＴ１３によって高周波交流電圧にいったん変換し、ＰチャンネルＦＥＴ１３のオン、オフ時間比を制御することにより電圧レベルを変えて、最終的に整流ダイオードＤ１、インダクタンスＬ１、コンデンサＣ１で構成された平滑回路を通じて、３．３Ｖ乃至５Ｖの直流電圧に変換する。

【０００４】このようなＤＣ－ＤＣコンバータ１１では、使用される機器の省電力化のために電力損失を小さくする必要があり、その改善策として図５に示すように、比較的電力損失の大きな整流ダイオードＤ１のかわりにＮチャンネルＦＥＴ１５を使用する方法が提案されている。この場合、ＮチャンネルＦＥＴ１５のゲートを発振回路１４に接続し、図６に示すように、ＮチャンネルＦＥＴ１５のドレイン－ソース間のパルスＱ２をＰチャンネルＦＥＴ１３のドレイン－ソース間のパルスＱ１に同期させて、ＰチャンネルＦＥＴ１３とＮチャンネルＦＥＴ１５が交互にスイッチングすることにより、ＮチャンネルＦＥＴ１５は整流器として働く。そして、ＮチャンネルＦＥＴ１５は、オン抵抗を低くすることが可能であるため、ＤＣ－ＤＣコンバータ１１の電力損失を大きく改善することができる。

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【０００５】

【発明が解決しようとする課題】しかしながら、実際にはＰチャンネルＦＥＴ１３及びＮチャンネルＦＥＴ１５は、駆動信号を印加されてからスイッチングするまでに数１０ｎ秒程度の遅延があり、このバラツキによってＰチャンネルＦＥＴ３とＮチャンネルＦＥＴ５がうまく同期せずに、同時にオンすることで地絡モードになり、電力損失がかえって増加してしまうという恐れがあった。

【０００６】それゆえ、本発明の主たる目的は、２つのスイッチング素子が同時にオンする状態を確実に防ぐスイッチング素子駆動回路を提供することである。

【０００７】

【課題を解決するための手段】上記の目的を達成するために、本発明は、２つのスイッチング素子を交互にスイッチングする同期式のスイッチング素子駆動回路において、幅制御された制御信号を発生する発振回路と、前記スイッチング素子の一方を駆動する第１の駆動信号を出力する論理和回路と、前記スイッチング素子の他方を駆動する第２の駆動信号を出力する論理積回路と、を備え、前記論理和回路の第１の駆動信号は前記発振回路の制御信号と前記論理積回路の第２の駆動信号とを論理和演算して生成し、前記論理積回路の第２の駆動信号は前記発振回路の制御信号と前記論理和回路の第１の駆動信号とを論理積演算して生成することにより、２つのスイッチング素子が同時にオンする状態を防ぐことを特徴とする。

【０００８】そして、前記論理和回路と前記論理積回路間に遅延回路を設けたことにより、前記スイッチング素子がスイッチするタイミングを調整したことを特徴とする。

【０００９】また、ＤＣ－ＤＣコンバータのスイッチング素子に使用したことを特徴とする。

【００１０】

【作用】上記の構成によれば、論理和回路と論理積回路を組み合わせることにより、２つのスイッチング素子が同時にオンする状態を防ぐことができる。また、論理和回路と前記論理積回路間に遅延回路を設けたことにより、スイッチング素子がスイッチするタイミングを調整することができる。

【００１１】

【実施例】以下、本発明のスイッチング素子駆動回路の一実施例を図面を用いて説明する。図１の回路図において、１は２つのスイッチング素子（図示せず）を交互に

スイッチングする同期式のスイッチング素子駆動回路、2は発振回路．3は論理和回路、4は論理積回路を示す。論理和回路3は一方の入力部が発振回路2と接続され．他方の入力部が論理積回路4の出力部と接続され、出力部が一方のスイッチング素子と接続される。論理積回路4は一方の入力部が発振回路2と接続され．他方の入力部が論理和回路3の出力部と接続され、出力部が他方のスイッチング素子と接続される。

【0012】このように構成されたスイッチング素子駆動回路1では．論理和回路3が発振回路2から発生される帽制御された制御信号Aと後述する論理積回路4の駆動信号Cを論理和演算することにより．駆動信号Bを出力して一方のスイッチング素子を駆動する。また．論理＊

＊積回路4が発振回路2の制御信号Aと論理和回路3の駆動信号Bを論理積演算することにより．駆動信号Cを出力して他方のスイッチング素子を駆動する。このような論理回路の組み合わせによれば、発振回路2の制御信号A．論理和回路3の駆動信号B、及び論理積回路4の駆動信号Cは、表1の真理値表に示すように、制御信号Aが0のときは駆動信号B及び駆動信号Cはともに0となり．制御信号Aが1のときは駆動信号B及び駆動信号Cはともに1となり、論理的には2つのスイッチング素子を完全に同期させることが可能となる。

【0013】

【表1】

A	B	C	B＝A＋C	C＝A×B	正・誤
0	0	0	0	0	○
0	0	1	1	0	○
0	1	0	0	0	×
0	1	1	1	0	×
1	0	0	1	0	×
1	0	1	1	0	×
1	1	0	1	1	×
1	1	1	1	1	○

【0014】次に、図5に示したDC－DCコンバータ11の発信回路14に変えて、スイッチング素子駆動回路1の論理和回路3の出力部とDC－DCコンバータ11のPチャンネルFET13のゲートを接続し．スイッチング素子駆動回路1の論理積回路4の出力部とDC－DCコンバータ11のNチャンネルFET15のゲートを接続した場合の実際のスイッチ動作について説明する。

【0015】図5に示したDC－DCコンバータ11は．PチャンネルFET13とNチャンネルFET15を同期させ、PチャンネルFET13とNチャンネルFET15が交互にスイッチングすることにより．電力損失の小さいDC－DCコンバータとして働く。しかしながら．PチャンネルFET13とNチャンネルFET15がうまく同期せずに同時にオンしてしまうと．かえって電力損失が増加することから、PチャンネルFET13とNチャンネルFET15が同時にオンする状態を確実に防ぐことが課題となっている。

【0016】図2のタイムチャート図には、スイッチング素子駆動回路1の発振回路2の制御信号A、論理和回路3の駆動信号B、及び論理積回路4の駆動信号C、並びに．DC－DCコンバータ11のPチャンネルFET13のドレイン－ソース間のパルスQ1、及びNチャンネルFET15のドレイン－ソース間のパルスQ2の各波形が示されている。

【0017】まず、A＝B＝C＝0の状態から．t，時点で．A＝1．B＝C＝0の状態となると、実際の半導体論理回路は入力信号に対して出力信号が数10n秒程度遅延することから、t₂時点でB＝A＋C＝1となる。そして、t₂時点で．A＝B＝1．C＝0の状態となると、t₂時点でC＝A×B＝1となる。

【0018】これにより．PチャンネルFET13のパルスQ1は、t₂時点で駆動信号B＝1が印加されてスイッチするが．駆動信号を印加されてからスイッチングするまでにも数十ナノ秒程度の遅延があることから、t₃時点でオンからオフにスイッチする。そして．NチャンネルFET15のパルスQ2も、t₃時点で駆動信号C＝1が印加されることにより、t₃時点でオフからオンにスイッチする。

【0019】次に、スイッチング素子駆動回路1は、A＝B＝C＝1の状態から．t₄時点で．A＝0．B＝C＝1の状態となると、t₇時点でC＝A×B＝0となる。そして、t₇時点で．A＝C＝0．B＝1の状態となり．t₈時点でB＝A＋C＝0となる。

【0020】これにより．NチャンネルFET15のパルスQ2は、t₇時点で駆動信号C＝0が印加されるこ

とにより、t_1時点でオンからオフにスイッチする。そして、PチャンネルFET13のパルスQ1も、t_6時点で駆動信号B＝0が印加されることにより、t_{10}時点でオフからオンにスイッチする。

【0021】この図2に示したPチャンネルFET13及びNチャンネルFET15のスイッチ動作からわかるように、実際にはt_2-t_1時点間でB＝1，C＝0になり、t_6-t_5時点間でB＝1，C＝0になるものの、それによって、PチャンネルFET13及びNチャンネルFET15はt_2-t_1時点間及びt_6-t_{10}時点間で同時にオフするだけで問題はなく、PチャンネルFET13及びNチャンネルFET15が同時にオンする状態になることはない。

【0022】しかし、PチャンネルFET13及びNチャンネルFET15の駆動信号を印加されてからスイッチングするまでのスイッチングスピードが異なることにより、t_2-t_1時点間及びt_6-t_5時点間が長くなる場合、或いはt_2-t_1時点間及びt_6-t_{10}時点間が短くなる場合は、PチャンネルFET13及びNチャンネルFET15が同時にオンする状態になる。そこで、このような場合には、図3に示すように、論理和回路3の他方の入力部と論理積回路4の出力部の間、及び論理積回路4の他方の入力部と論理和回路3の出力部の間に遅延回路5を設けることで、PチャンネルFET13及びNチャンネルFET15の駆動信号を印加されてからスイッチングするまでの遅延時間のバラツキを調整することができる。

【0023】また、このスイッチング素子駆動回路1は回路構成が簡単なことから安価で製造でき、低コストで確実なスイッチング素子の同期スイッチングが可能な高効率のDC－DCコンバータを実現できる。なお、上述の実施例では、MOS形FETを使用して説明したが、＊接合形FETなど、他のどのようなスイッチング素子でもよく、利用分野はDC－DCコンバータに限らない。

【0024】

【発明の効果】以上説明したように、本発明にかかるスイッチング素子駆動回路によれば、論理回路の組み合わせにより、2つのFETが同時にオンする状態を防ぐことができ、遅延回路を加えたことで、前記スイッチング素子がスイッチするタイミングを調整することができる。また、回路構成が簡単なことから安価で製造でき、低コストで確実なスイッチング素子の同期スイッチングが可能となる。さらに、当該スイッチング素子駆動回路をDC－DCコンバータに用いることにより、DC－DCコンバータの電力損失を小さくする効果がある。

【図面の簡単な説明】

【図1】本発明の実施例におけるスイッチング素子駆動回路を示す回路図である。

【図2】図1のスイッチング素子駆動回路の各部波形を示したタイムチャート図である。

【図3】図1のスイッチング素子駆動回路に遅延回路を加えた状態を示す回路図である。

【図4】整流ダイオードを備えた従来のDC－DCコンバータを示す回路図である。

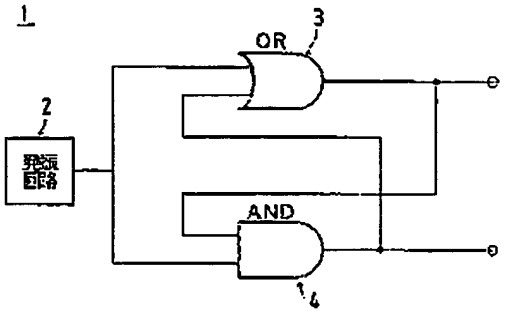
【図5】図1のDC－DCコンバータの整流ダイオードをMOS形FETに変えた状態を示す回路図である。

【図6】図5のDC－DCコンバータの各部波形を示したタイムチャート図である。

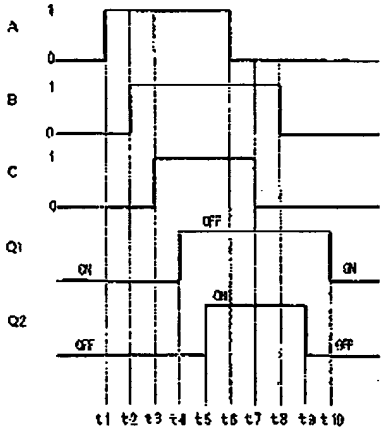
【符号の説明】

1　スイッチング素子駆動
2　発振回路
3　論理和回路
4　論理積回路
5　遅延回路

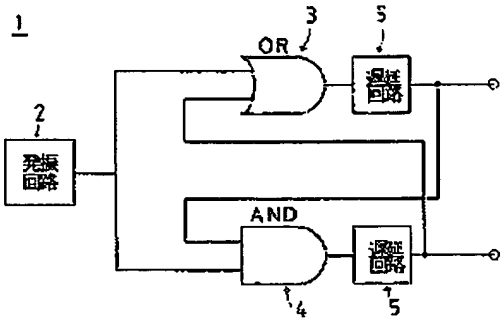
【図1】



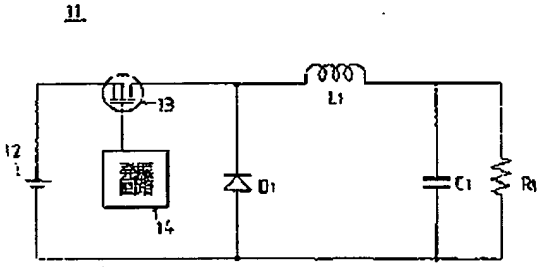
【図2】



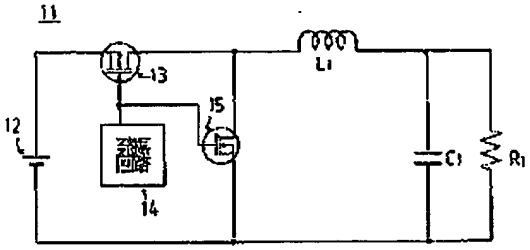
【図3】


1
2
発振回路
3
OR
5
遅延回路
AND
4
5

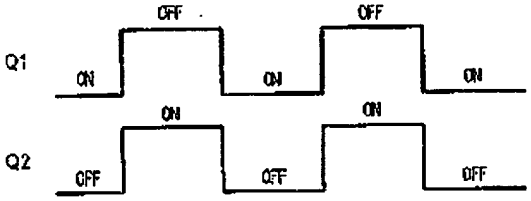
【図4】


11
13
L1
12
発振回路
14
D1
C1
R1

【図5】


11
13
L1
15
12
発振回路
14
C1
R1

【図6】


Q1
Q2
ON
OFF
ON
OFF
ON
OFF
ON
OFF
ON
OFF

Japanese Patent Application Publication No. 08-018419

CLAIMS

[Claim(s)]

[Claim 1] In a switching element actuation circuit of synchronous system which switches two switching elements by turns An oscillator circuit which generates a control signal by which width-of-face control was carried out, and an OR circuit which outputs the 1st driving signal which drives one side of said switching element, An AND circuit which outputs the 2nd driving signal which drives another side of said switching element, The 1st driving signal of a preparation and said OR circuit carries out OR operation of a control signal of said oscillator circuit, and the 2nd driving signal of said AND circuit, and generates them. By carrying out the AND operation of a control signal of said oscillator circuit, and the 1st driving signal of said alternation gate, and generating them, the 2nd driving signal of said AND circuit is a switching element actuation circuit characterized by preventing the condition that two switching elements turn on simultaneously.

[Claim 2] A switching element actuation circuit according to claim 1 characterized by adjusting timing which said switching element switches by having prepared a delay circuit between said alternation gates and said AND circuits.

[Claim 3] Claim 1 characterized by using it for a switching element of a DC-DC converter, and a switching element actuation circuit according to claim 2.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the switching element actuation circuit used for a DC-DC converter, concerning a switching element actuation circuit.
[0002]
[Description of the Prior Art] DC power supply are considered as an input and the basic circuit of the DC-DC converter of the pressure-lowering chopper mold which outputs the stable direct current voltage is shown in drawing 4 . drawing 4 -- setting -- 11 -- a DC-DC converter and 12 -- direct-current input power and 13 -- in P channel FET of an MOS form, and 14, an inductance and C1 show a capacitor and, as for an oscillator circuit and D1, R1 shows a load, as for rectifier diode and L1.
[0003] DC-DC converter 11 once changes the direct current voltage of the direct-current input power 12 into RF alternating voltage by P channel FET13 which impressed the driving signal of an oscillator circuit 14, by controlling ON of P channel FET13, and an off time amount ratio, changes a voltage level and changes it into the direct current voltage of 3.3V thru/or 5V through the smoothing circuit which consisted of rectifier diode D1, an inductance L1, and a capacitor C1 eventually.
[0004] It is necessary to make power loss small for power-saving of the device used, and in such DC-DC converter 11, as shown in drawing 5 as the remedy, the method of using the N channel FET 15 instead of the rectifier diode D1 with comparatively big power loss is proposed. In this case, as it connects with an oscillator circuit 14 and the gate of the N channel FET 15 is shown in drawing 6 , when the pulse Q2 between the drain-sources of the N channel FET 15 is synchronized with the pulse Q1 between the drain-sources of P channel FET13 and P channel FET13 and the N channel FET 15 switch by turns, the N channel FET 15 works as a rectifier. And since the N channel FET 15 can make on resistance low, the power loss of DC-DC converter 11 is greatly improvable.
[0005]
[Problem(s) to be Solved by the Invention] however -- before [after a driving signal is actually impressed to P channel FET13 and the N channel FET 15] switching -- several 10 -- there was delay of an about [n second], it became ground mode by turning on simultaneously, without P channel FET3 and the N channel FET 5 synchronizing well by this variation, and there was a possibility that power loss may increase on the contrary.
[0006] So, the main object of this invention is offering the switching element actuation circuit which prevents certainly the condition two switching elements' turning on simultaneously.
[0007]
[Means for Solving the Problem] In a switching element actuation circuit of synchronous system with which this invention switches two switching elements by turns in order to attain the above-mentioned object An oscillator circuit which generates a control signal by which width-of-face control was carried out, and an OR circuit which outputs the 1st driving signal which drives one side of said switching element, An AND circuit which outputs the 2nd driving signal which drives another side of said switching element, The 1st driving signal of a preparation and said OR circuit carries out OR operation of a control signal of said oscillator circuit, and the 2nd driving signal of said AND circuit, and generates them. It is characterized by the 2nd driving

signal of said AND circuit preventing the condition that two switching elements turn on simultaneously by carrying out the AND operation of a control signal of said oscillator circuit, and the 1st driving signal of said alternation gate, and generating them.
[0008] And it is characterized by adjusting timing which said switching element switches by having prepared a delay circuit between said alternation gates and said AND circuits.
[0009] Moreover, it is characterized by using it for a switching element of a DC-DC converter.
[0010]
[Function] According to the above-mentioned configuration, two switching elements can prevent the condition of turning on simultaneously, by combining an alternation gate and an AND circuit. Moreover, the timing which a switching element switches can be adjusted by having prepared the delay circuit between the alternation gate and said AND circuit.
[0011]
[Example] Hereafter, one example of the switching element actuation circuit of this invention is explained using a drawing. In the circuit diagram of drawing 1 , in the switching element actuation circuit of the synchronous system with which 1 switches two switching elements (not shown) by turns, and 2, an oscillator circuit and 3 show an OR circuit and 4 shows an AND circuit. One input section is connected with an oscillator circuit 2, the input section of another side is connected with the output section of AND circuit 4, and, as for OR circuit 3, the output section is connected with one switching element. One input section is connected with an oscillator circuit 2, the input section of another side is connected with the output section of an alternation gate 3, and, as for AND circuit 4, the output section is connected with the switching element of another side.
[0012] Thus, in the constituted switching element actuation circuit 1, when OR circuit 3 carries out OR operation of the control signal A which is generated from an oscillator circuit 2 and by which width-of-face control was carried out, and the driving signal C of AND circuit 4 mentioned later, a driving signal B is outputted and one switching element is driven. Moreover, when AND circuit 4 carries out the AND operation of the control signal A of an oscillator circuit 2, and the driving signal B of OR circuit 3, a driving signal C is outputted and the switching element of another side is driven. According to the combination of such a logical circuit, the control signal A of an oscillator circuit 2, the driving signal B of OR circuit 3, and the driving signal C of AND circuit 4 As shown in the table of truth value of a table 1, when a control signal A is 0, both the driving signal B and the driving signal C are set to 0, when a control signal A is 1, both the driving signal B and the driving signal C are set to 1, and it becomes possible to synchronize two switching elements thoroughly logically.
[0013]
[A table 1]
[0014] Next, actual switching at the time of changing into the dispatch circuit 14 of DC-DC converter 11 shown in drawing 5 , connecting the gate of P channel FET13 of DC-DC converter 11 with the output section of the alternation gate 3 of the switching element actuation circuit 1, and connecting the gate of the N channel FET 15 of DC-DC converter 11 with the output section of AND circuit 4 of the switching element actuation circuit 1 is explained.
[0015] DC-DC converter 11 shown in drawing 5 works as a small DC-DC converter of power loss, when P channel FET13 and the N channel FET 15 are synchronized and P channel FET13 and the N channel FET 15 switch by turns. However, after P channel FET13 and the N channel FET 15 turn on simultaneously, without synchronizing well, since power loss increases on the contrary, it has been a technical problem to prevent certainly the condition that P channel FET13

and the N channel FET 15 turn on simultaneously.
[0016] Each wave of the pulse Q1 between the drain-sources of P channel FET13 of DC-DC converter 11 and the pulse Q2 between the drain-sources of the N channel FET 15 is shown in timing diagram drawing of drawing 2 at the control signal A, the driving signal B of an alternation gate 3 and the driving signal C of AND circuit 4, and list of an oscillator circuit 2 of the switching element actuation circuit 1.
[0017] First, the condition of A=B=C=0 to t1 When it will be in the condition of A= 1 and B=C=0 at the event, a actual semiconductor logical circuit is t2 since an output signal carries out several 10n second grade delay to an input signal. It is set to B=A+C=1 at the event. And t2 It is t3 when it will be in the condition of A=B=1 and C= 0 at the event. It is set to C=AxB=1 at the event.
[0018] Thereby, the pulse Q1 of P channel FET13 is t2. t4 since there is delay for about dozens of nanoseconds after a driving signal is impressed also before switching although a driving signal B= 1 is impressed and being switched at the event It switches off from ON at the event. And the pulse Q2 of the N channel FET 15 is also t3. By impressing a driving signal C= 1 at the event, it is t5. It switches to ON from OFF at the event.
[0019] Next, the switching element actuation circuit 1 is the condition of A=B=C=1 to t6. It is t7 when it will be in the condition of A= 0 and B=C=1 at the event. It is set to C=AxB=0 at the event. And t7 At the event, it will be in the condition of A=C=0 and B= 1, and is t8. It is set to B=A+C=0 at the event.
[0020] Thereby, the pulse Q2 of the N channel FET 15 is t7. By impressing a driving signal C= 0 at the event, it is t9. It switches off from ON at the event. And the pulse Q1 of P channel FET13 is also t8. By impressing a driving signal B= 0 at the event, it switches to ON from OFF at the t10 event.
[0021] So that switching of the P channel FET13 and the N channel FET 15 which were shown in this drawing 2 may show actual -- t2-t3 an event -- between -- it is -- B= 1 and C= 0 -- becoming -- t6-t7 an event -- between -- it is -- B= -- by it, although set to 1 and C= 0 P channel FET13 and the N channel FET 15 -- t4-t5 an event -- between -- and -- t -- nine - t -- ten -- an event -- between -- it is -- simultaneous -- turning off -- only -- a problem -- there is nothing -- P -- a channel -- FET -- 13 -- and -- N -- a channel -- FET -- 15 -- simultaneous -- turning on -- a condition -- becoming -- things -- there is nothing .
[0022] However, when switching speed after the driving signal of P channel FET13 and the N channel FET 15 is impressed until it switches differs t2-t4 an event -- between and t7-t9 an event -- between -- long -- becoming -- a case -- or -- t -- 3 -- - -- t5 an event -- between -- and -- t -- eight -- - -- t -- ten -- < -- /-- SUB -- > -- an event -- between -- short -- becoming -- a case -- P -- a channel -- FET -- 13 -- and -- N -- a channel -- FET -- 15 -- simultaneous -- turning on -- a So, in such a case, as shown in drawing 3 , the variation in a time delay after the driving signal of P channel FET13 and the N channel FET 15 is impressed until it switches can be adjusted by forming a delay circuit 5 between the input section of another side of OR circuit 3, and the output section of AND circuit 4, and between the input section of another side of AND circuit 4, and the output section of OR circuit 3.
[0023] Moreover, from circuitry being easy, this switching element actuation circuit 1 can be cheap, and can be manufactured, and the efficient DC-DC converter in which synchronous switching of a positive switching element is possible can be realized by low cost. In addition, in the above-mentioned example, although explained using the MOS FET, a switching element like other throats is sufficient as a junction type FET etc., and a field of the invention does not restrict

it to a DC-DC converter.

[0024]

[Effect of the Invention] As explained above, according to the switching element actuation circuit concerning this invention, with the combination of a logical circuit, the condition that two FET turns on simultaneously can be prevented and the timing which said switching element switches can be adjusted by having added the delay circuit. Moreover, from an easy thing, circuitry is cheap, and can manufacture, and synchronous switching of a positive switching element of it becomes possible by low cost. Furthermore, there is an effect which makes power loss of a DC-DC converter small by using the switching element actuation circuit concerned for a DC-DC converter.

TECHNICAL FIELD

[Industrial Application] This invention relates to the switching element actuation circuit used for a DC-DC converter, concerning a switching element actuation circuit.

PRIOR ART

[Description of the Prior Art] DC power supply are considered as an input and the basic circuit of the DC-DC converter of the pressure-lowering chopper mold which outputs the stable direct current voltage is shown in drawing 4 . drawing 4 -- setting -- 11 -- a DC-DC converter and 12 -- direct-current input power and 13 -- in P channel FET of an MOS form, and 14, an inductance and C1 show a capacitor and, as for an oscillator circuit and D1, R1 shows a load, as for rectifier diode and L1.

[0003] DC-DC converter 11 once changes the direct current voltage of the direct-current input power 12 into RF alternating voltage by P channel FET13 which impressed the driving signal of an oscillator circuit 14, by controlling ON of P channel FET13, and an off time amount ratio, changes a voltage level and changes it into the direct current voltage of 3.3V thru/or 5V through the smoothing circuit which consisted of rectifier diode D1, an inductance L1, and a capacitor C1 eventually.

[0004] It is necessary to make power loss small for power-saving of the device used, and in such DC-DC converter 11, as shown in drawing 5 as the remedy, the method of using the N channel FET 15 instead of the rectifier diode D1 with comparatively big power loss is proposed. In this case, as it connects with an oscillator circuit 14 and the gate of the N channel FET 15 is shown in drawing 6 , when the pulse Q2 between the drain-sources of the N channel FET 15 is synchronized with the pulse Q1 between the drain-sources of P channel FET13 and P channel FET13 and the N channel FET 15 switch by turns, the N channel FET 15 works as a rectifier. And since the N channel FET 15 can make on resistance low, the power loss of DC-DC converter 11 is greatly improvable.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, according to the switching element actuation circuit concerning this invention, with the combination of a logical circuit, the condition that two FET turns on simultaneously can be prevented and the timing which said switching element switches can be adjusted by having added the delay circuit. Moreover, from an easy thing, circuitry is cheap, and can manufacture, and synchronous switching of a positive switching element of it becomes possible by low cost. Furthermore, there is an effect which makes power loss of a DC-DC converter small by using the switching element actuation circuit concerned for a DC-DC converter.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] however -- before [after a driving signal is actually impressed to P channel FET13 and the N channel FET 15] switching -- several 10 -- there was delay of an about [n second], it became ground mode by turning on simultaneously, without P channel FET3 and the N channel FET 5 synchronizing well by this variation, and there was a possibility that power loss may increase on the contrary.

[0006] So, the main object of this invention is offering the switching element actuation circuit which prevents certainly the condition two switching elements' turning on simultaneously.

MEANS

[Means for Solving the Problem] In a switching element actuation circuit of synchronous system with which this invention switches two switching elements by turns in order to attain the above-mentioned object An oscillator circuit which generates a control signal by which width-of-face control was carried out, and an OR circuit which outputs the 1st driving signal which drives one side of said switching element, An AND circuit which outputs the 2nd driving signal which drives another side of said switching element, The 1st driving signal of a preparation and said OR circuit carries out OR operation of a control signal of said oscillator circuit, and the 2nd driving signal of said AND circuit, and generates them. It is characterized by the 2nd driving signal of said AND circuit preventing the condition that two switching elements turn on simultaneously by carrying out the AND operation of a control signal of said oscillator circuit, and the 1st driving signal of said alternation gate, and generating them.
[0008] And it is characterized by adjusting timing which said switching element switches by having prepared a delay circuit between said alternation gates and said AND circuits.
[0009] Moreover, it is characterized by using it for a switching element of a DC-DC converter.

OPERATION

[Function] According to the above-mentioned configuration, two switching elements can prevent the condition of turning on simultaneously, by combining an alternation gate and an AND circuit. Moreover, the timing which a switching element switches can be adjusted by having prepared the delay circuit between the alternation gate and said AND circuit.

EXAMPLE

[Example] Hereafter, one example of the switching element actuation circuit of this invention is explained using a drawing. In the circuit diagram of drawing 1 , in the switching element actuation circuit of the synchronous system with which 1 switches two switching elements (not shown) by turns, and 2, an oscillator circuit and 3 show an OR circuit and 4 shows an AND circuit. One input section is connected with an oscillator circuit 2, the input section of another side is connected with the output section of AND circuit 4, and, as for OR circuit 3, the output section is connected with one switching element. One input section is connected with an oscillator circuit 2, the input section of another side is connected with the output section of an alternation gate 3, and, as for AND circuit 4, the output section is connected with the switching element of another side.

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[0013]

[A table 1]

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[0016] Each wave of the pulse Q1 between the drain-sources of P channel FET13 of DC-DC converter 11 and the pulse Q2 between the drain-sources of the N channel FET 15 is shown in timing diagram drawing of drawing 2 at the control signal A, the driving signal B of an alternation gate 3 and the driving signal C of AND circuit 4, and list of an oscillator circuit 2 of the switching element actuation circuit 1.

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t3 when it will be in the condition of A=B=1 and C= 0 at the event. It is set to C=AxB=1 at the event.
[0018] Thereby, the pulse Q1 of P channel FET13 is t2. t4 since there is delay for about dozens of nanoseconds after a driving signal is impressed also before switching although a driving signal B= 1 is impressed and being switched at the event It switches off from ON at the event. And the pulse Q2 of the N channel FET 15 is also t3. By impressing a driving signal C= 1 at the event, it is t5. It switches to ON from OFF at the event.
[0019] Next, the switching element actuation circuit 1 is the condition of A=B=C=1 to t6. It is t7 when it will be in the condition of A= 0 and B=C=1 at the event. It is set to C=AxB=0 at the event. And t7 At the event, it will be in the condition of A=C=0 and B= 1, and is t8. It is set to B=A+C=0 at the event.
[0020] Thereby, the pulse Q2 of the N channel FET 15 is t7. By impressing a driving signal C= 0 at the event, it is t9. It switches off from ON at the event. And the pulse Q1 of P channel FET13 is also t8. By impressing a driving signal B= 0 at the event, it switches to ON from OFF at the t10 event.
[0021] So that switching of the P channel FET13 and the N channel FET 15 which were shown in this drawing 2 may show actual -- t2-t3 an event -- between -- it is -- B= 1 and C= 0 -- becoming -- t6-t7 an event -- between -- it is -- B= -- by it, although set to 1 and C= 0 P channel FET13 and the N channel FET 15 -- t4-t5 an event -- between -- and -- t -- nine - t -- ten -- an event -- between -- it is -- simultaneous -- turning off -- only -- a problem -- there is nothing -- P -- a channel -- FET -- 13 -- and -- N -- a channel -- FET -- 15 -- simultaneous -- turning on -- a condition -- becoming -- things -- there is nothing .
[0022] however, the thing which switching speed after the driving signal of P channel FET13 and the N channel FET 15 is impressed until it switches differs -- t2-t4 an event -- between and t7-t9 an event -- between -- long -- becoming -- a case -- or -- t -- 3 -- - -- t5 an event -- between - - and -- t -- eight -- - -- t -- ten -- an event -- between -- short -- becoming -- a case -- P -- a channel -- FET So, in such a case, as shown in drawing 3 , the variation in a time delay after the driving signal of P channel FET13 and the N channel FET 15 is impressed until it switches can be adjusted by forming a delay circuit 5 between the input section of another side of OR circuit 3, and the output section of AND circuit 4, and between the input section of another side of AND circuit 4, and the output section of OR circuit 3.
[0023] Moreover, from circuitry being easy, this switching element actuation circuit 1 can be cheap, and can be manufactured, and the efficient DC-DC converter in which synchronous switching of a positive switching element is possible can be realized by low cost. In addition, in the above-mentioned example, although explained using the MOS FET, a switching element like other throats is sufficient as a junction type FET etc., and a field of the invention does not restrict it to a DC-DC converter.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram showing the switching element actuation circuit in the example of this invention.
[Drawing 2] It is timing diagram drawing having shown each part wave of the switching element actuation circuit of drawing 1 .
[Drawing 3] It is the circuit diagram showing the condition of having added the delay circuit to the switching element actuation circuit of drawing 1 .
[Drawing 4] It is the circuit diagram showing the conventional DC-DC converter equipped with rectifier diode.
[Drawing 5] It is the circuit diagram showing the condition of having changed the rectifier diode of the DC-DC converter of drawing 1 into the MOS FET.
[Drawing 6] It is timing diagram drawing having shown each part wave of the DC-DC converter of drawing 5 .
[Description of Notations]
1 Switching Element Actuation
2 Oscillator Circuit
3 OR Circuit
4 AND Circuit
5 Delay Circuit